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Our Docket No.: 98-197/1C / 1496.00065 10/24/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	Jackson L. Ellis et al.		
Application No.:	09/183,694	Examiner:	Park, I.
Filed:	October 30, 1998	Art Group:	2182
For:	COMMAND QUEUEING ENGINE		

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on October 23, 2002.

By: Mary Donna Berkley
Mary Donna Berkley

APPEAL BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for consideration by the Board of Patent Appeals and Interferences. Please charge $320.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(f) and any additional fees or credit any overpayment to Deposit Account Number 12-2252.

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, LSI Logic Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 3 and 16-26 are pending and remain rejected. The Appellants hereby appeal the rejection of claims 3 and 16-26.

IV. STATUS OF AMENDMENTS

Appellants are appealing a Final Office Action issued by the Examiner on June 18, 2002. On July 25, 2002, Appellants filed a Response After Final requesting reconsideration without amending the claims. On August 5, 2002, an Advisory Action was mailed that maintained the rejections and removed an admission in the June 18, 2002 Final Office Action regarding claim 21. On September 18, 2002, Appellants filed a Notice of Appeal.

V. SUMMARY OF INVENTION

The present invention concerns a data controller (150) that is couplable to a host (120) and coupled to a storage medium (130), microprocessor (160), local storage (190) and a buffer

memory (170), comprising a command queuing engine (215) that creates a plurality of threads of sequential commands that exist simultaneously (TCB 1, TCB 2 and TCB 3 in FIG. 9) while minimizing interrupts associated to the commands (1205, 1210 and 1215).

VI. ISSUES

The issue is whether (i) claims 21, 22 and 26 are patentable under 35 U.S.C. §102(e) over Krakirian, U.S. Patent No. 5,781,803, (ii) claim 3 is patentable under 35 U.S.C. §103(a) over Krakirian in view of Jones et al., U.S. Patent No. 5,483,641, (iii) claims 16-20 are patentable under 35 U.S.C. §103(a) over Krakirian in view of Jones et al. and in further view of Bean et al., U.S. Patent No. 4,543,626, and (iv) claims 23-25 are patentable under 35 U.S.C. §103(a) over Krakirian in view of Bean et al.

VII. GROUPING OF CLAIMS

Appellants contend that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1: Claims 21 and 22 stand together

Group 2: Claim 26 stands alone.

Group 3: Claim 3 stands alone.

Group 4: Claims 16-20 stand together.

Group 5: Claims 23-25 stand together.

The claim(s) in each group is (are) separately patentable from the claim(s) in any other groups.

VIII. ARGUMENTS

A. 35 U.S.C. § 102

The Federal Circuit has stated that "[t]o anticipate, *every element and limitation* of the claimed invention must be found in a single prior art reference, *arranged as in the claim.*"[1] (Emphasis added). The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[2]

Selected groupings of the claims are each patentable over Krakirian

1. Group 1 (Claims 21 and 22) are fully patentable over Krakirian.

A conclusion of anticipation for the above-cited claims cannot be supported because Krakirian does not appear to disclose or suggest (a) a data controller that minimizes interrupts to a processor, (b) by reordering a plurality of commands received from a host computer. Krakirian discloses a system for storing initiator, queue tag, and logical block information, disconnecting from target if command is not auto transfer, reconnecting and performing data transfer (Title).

Pending claim 21 provides a data controller that minimizes interrupts to a processor by reordering a plurality of commands received from a host computer. In contrast, the Examiner has stated, "However Krakirian *does not explicitly disclose* the data controller minimizes interrupts to

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[1] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant).

[2] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

the processor by the reordering."[3] (emphasis added). The statement is an admission that Krakirian does not disclose every element as arranged in claim 21. The admission was later withdrawn by the Examiner because it has "*nothing to do with the claim* and should be deleted."[4] (emphasis added). Appellants' representative respectfully disagrees that the statement has nothing to do with the claim. The pending claim 21 provides minimizing interrupts to a processor by reordering which is the subject of the statement. Since the statement is being withdrawn on a false reason, the statement should be allowed to stand. Therefore, the Examiner has admitted that (item 1) Krakirian does not disclose or suggest a data controller that minimizes interrupts to a processor by reordering a plurality of commands received from a host computer as presently claimed.

Assuming, *arguendo*, that the statement was made in error and should be withdrawn (for which the Appellants' representative does not necessarily agree), Krakirian does not appear to disclose or suggest that the reordering of a plurality of commands is performed by a data controller. In particular, the Examiner has cited a hard disk controller IC 204 of Krakirian has the claimed data controller.[5] However, Krakirian states that a target device 202 may reorder the commands.[6] While the target device 202 of Krakirian contains the hard disk controller IC 204 cited by the Examiner, the target device 202 also contains other elements capable of reordering, such as a microprocessor 206. Krakirian appears silent regarding which element or elements within the target device 202 provide the reordering function. Any allocation of the reordering function only to the hard disk

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[3] Office Action, June 18, 2002, page 3, item 5, lines 8-9.

[4] Advisory Action, August 5, 2002, page 2, line 5.

[5] Office Action, June 18, 2002, page 3, item 5, line 3.

[6] Krakirian, column 15, lines 23-24.

controller IC 204 is pure speculation. Therefore, Krakirian does not appear to disclose or suggest (item 2) a data controller that reorders a plurality of commands received from a host computer as presently claimed.

Furthermore, pending claim 21 provides that the data controller minimizes interrupts to a processor. The Examiner has cited Krakirian for minimizing interrupts to a microprocessor 206.[7] The first paragraph of the cited text of Krakirian reads:[8]

> Not only does the SCSI interface portion 211 of the disk controller integrated circuit 204 proceed from the command bus phase to the data transfer bus phase without waiting for a *communication from the microprocessor* for commands determined to be autowrite commands, but the SCSI interface portion 211 also proceeds from the command bus phase to the data transfer bus phase without waiting for a *communication from the microprocessor* for commands called "ESP commands". Note that execution of the B_AUTO command at location 13h in FIG. 7A also causes the sequence to proceed to the data transfer sequencer (denoted XFR sequence in FIG. 7A) if the ESP bit of register HSTAT0 (OCh) is set. In a command determined to be an ESP command, the logical block address of the command matches an expected logical block address which was previously loaded by microprocessor 206 into four registers HESPLBA0, HESPLBA1, HESPLBA2 and HESPLBA3 (3Ch-3Fh). (Emphasis added)

The remaining two paragraphs of the cited text do not mention the microprocessor 206. Krakirian discloses proceeding without waiting for *communications from* the microprocessor 206, not minimizing *interrupts to* a microprocessor as presently claimed. Krakirian also appears to suggest that the microprocessor 206 is interrupted upon receipt of each command:[9]

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[7] Office Action, June 18, 2002, page 3, item 5, lines 5-7.

[8] Krakirian, column 16, lines 34-51.

[9] Krakirian, column 12 lines 35-40.

> The CDB parsing state machine parses the command, loads information from different fields of the command into corresponding other CFIFO locations and *then generates an interrupt to the microprocessor to notify the microprocessor 206 that a new command has been received and parsed.* (Emphasis added)

To test for a valid queue tag in each command, Krakirian states, "Accordingly, after CFIFO 217 is initially loaded with the queue tag information for the received command, *microprocessor 206 receives the CDBDONE interrupt and then reads the queue tag.*" (emphasis added).[10] For "autotransfer" type commands, at least two interrupts may be generated for each command:[11]

> In accordance with some embodiments of the present invention, an autotransfer command (such as an autoread or an autowrite command) is carried out by the disk drive controller integrated circuit with only *two interrupts being generated to the microprocessor:* one after receiving the autotransfer command from the initiator; and one after the data transfer of the autotransfer command is complete. (Emphasis added)

In some cases, more than two interrupts may be generated per autotransfer command, "Moreover, in some embodiments, a microprocessor may be interrupted more than two times for the execution of an autotransfer command."[12] Krakirian appears to disclose that the microprocessor 206 is interrupted for each command received. Therefore, Krakirian does not appear to disclose or suggest (item 3) a data controller that minimizes interrupts to a processor as presently claimed.

In summary, (item 1) the Examiner has conceded, at least until after Appellants final response was submitted, that Krakirian does not disclose or suggest a data controller that minimizes

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[10] Krakirian, column 15, lines 35-38.

[11] Krakirian, column 5, lines 27-33.

[12] Krakirian, column 21, lines 46-49.

interrupts to a processor by reordering. Furthermore, Krakirian does not appear to disclose or suggest (item 2) a data controller that reorders a plurality of commands received from a host computer and (item 3) a data controller that minimizes interrupts to a processor as presently claimed. Therefore, the pending claim 21 is fully patentable over Krakirian and the rejection should be reversed.

2. Group 2 (Claim 26) is fully patentable over Krakirian.

A conclusion of anticipation for the above-cited claim cannot be supported because Krakirian does not appear to disclose or suggest a data controller that creates threads of a plurality of commands. Krakirian discloses a system for storing initiator, queue tag, and logical block information, disconnecting from target if command is not auto transfer, reconnecting and performing data transfer (Title).

Pending claim 26 provides a peripheral device that includes a data controller that creates threads of a plurality of commands. Despite the citations provided by the Examiner, Krakirian does not appear to disclose or suggest the claimed invention.[13] In particular, Krakirian is cited as disclosing a creation of threads (plural). The cited text of Krakirian reads, "Multiple commands are therefore 'queued' in the target provided that no two outstanding commands received from a single initiator have the same queue ID tag."[14] The cited text of Krakirian appears to disclose a queue. The cited text and the remaining text of Krakirian appears to be silent regarding the queue holding several threads of commands. One does not anticipate plural, therefore Krakirian does not

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[13] Office Action, June 18, 2002, page 3, item 5, lines 12-17.

[14] Krakirian, column 15, lines 27-29.

appear to disclose or suggest (item 4) a data controller that creates threads of a plurality of commands as presently claimed.

Furthermore, the Examiner has conceded that Krakirian does not disclose of suggest that the queue may hold multiple threads simultaneously, "However, Krakirian *does not explicitly disclose* the plurality of threads of sequential commands exist simultaneously." (emphasis added).[15] While a queue may hold a single thread, Krakirian does not appear to disclose or suggest that the queue can hold multiple threads and (item 5) the Examiner has admitted that the queue of Krakirian cannot hold plural threads simultaneously. Therefore, Krakirian does not appear to disclose or suggest a peripheral device that includes a data controller that creates threads of a plurality of commands as presently claimed.

In summary, Krakirian does not appear to disclose or suggest (item 4) a data controller that creates threads of a plurality of commands as presently claimed and (item 5) the Examiner has admitted that the queue disclosed by Krakirian cannot hold plural threads simultaneously. As such, the pending claim 26 is fully patentable over the cited reference and the rejection should be reversed.

B. **35 U.S.C. § 103**

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the

[15] Office Action, June 18, 2002, page 4, item 7, lines 7-8.

specific combination that was made by the applicants."[16] "[T]he factual inquiry whether to combine references must be thorough and searching."[17] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[18] "It must be based on objective evidence of record."[19] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.[20]

Selected groupings of the claims are each patentable over Krakirian in view of Jones et al.

1. Group 3 (Claim 3) is fully patentable over Krakirian in view of Jones et al.

A prima facie case has not established that it would have been obvious to one of ordinary skill in the art to modify the teaching of Krakirian with the teaching of Jones et al. In particular, (a) the burden of proof has not been meet to show motivation to modify Krakirian with Jones et al. and (b) the suggested modification does not appear to teach or suggest all of the claim

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[16] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[17] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[18] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[19] *Id.* at 1343, 61 USPQ2d at 1434.

[20] M.P.E.P. §2142.

limitations as arranged in pending claim 3. Krakirian teaches a system for storing initiator, queue tag, and logical block information, disconnecting from target if command is not auto transfer, reconnecting and performing data transfer (Title). Jones et al. teach a system for scheduling read ahead operations if new request is within a proximity of N last read requests wherein N is dependent on independent activities (Title).

The show motivation to combine the references, the Examiner has argued that (a) both Krakirian and Jones et al. teach creating a plurality of threads of sequential commands and (b) modifying Krakirian with Jones et al. would increase flexibility in handling multiple SCSI commands.[21] In contrast, the Examiner had previously admitted that Krakirian does not explicitly disclose that the plurality of threads of sequential commands exist simultaneously, "However, Krakirian *does not explicitly disclose* the plurality of threads of sequential commands exist simultaneously." (emphasis added).[22] Therefore, the first argument for motivation to combine the references appears to be false.

The second motivation to combine the references would be to increase flexibility in handling multiple SCSI commands. Such a conclusory statement alone is not thorough and searching evidence for motivation. Krakirian already teaches handling of multiple commands through a queue.[23] No evidence has been provided why one of ordinary skill in the art would believe that the apparatus taught by Krakirian should have an increased queuing flexibility. No evidence has been provided why one of ordinary skill in the art would seek Jones et al. in particular to

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[21] Office Action, June 18, 2002, page 4, item 7 line 12 through page 5 line 2.

[22] Office Action, June 18, 2002, page 4, item 7, lines 7-8.

[23] Krakirian, column 15, lines 27-29.

increase a flexibility of the queuing already taught by Krakirian. Finally, no evidence has been provided that the teachings of Jones et al. would have a reasonable expectation of success to increase the queuing flexibility of the Krakirian invention.

Furthermore, the United States patent laws allow improvements to existing inventions to be patented.[24] A desire to improve an invention alone is not sufficient motivation to make a combination obvious. Therefore, (item 6) a prima facie case of obviousness to combine Krakirian and Jones et al. has not been established for lack of motivation.

Assuming, arguendo, that it would have been obvious to combine the teachings of Krakirian and Jones et al. (for which the Appellants' representative does not agree), the combination still does not teach or suggest every element as arranged in the pending claim 3. Pending claim 3 provides a data control having a command queuing engine that creates a plurality of threads of sequential commands that exist simultaneously. In contrast, the Examiner has conceded that Krakirian does not disclose of suggest that the queue may hold multiple threads simultaneously.[25] Examiner has cited two places in Jones et al. as teaching creation of a plurality of threads of sequential commands that exist simultaneously.[26] However, the first cited text of Jones et al. reads:[27]

> Read/Write Combining
> When multiple sequential read or write requests exist on the drive queue, DDA will combine those requests into *single, large requests* to enhance performance. This is

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[24] 35 U.S.C. §101.

[25] Office Action, June 18, 2002, page 4, item 7, lines 7-8.

[26] Office Acton, June 18, 2002, page 4, item 7, lines 9-11.

[27] Jones et al., column 50, lines 50-60.

> especially effective for small writes on guarded arrays. If an error occurs, the requests are decombined and run as ORIGINALs to simplify error handling. In the following example, multiple, sequential disk reads are enqueued. The composite drive type is unimportant, but the maximum transfer size of the composite disk is 128. (Emphasis added)

Jones et al. appear to teach combining multiple requests into a single request. Creating a single request does not teach or suggest creating multiple threads of commands that exist simultaneously as presently claimed.

The second cited text of Jones et al. provides several snapshots of a queue during a guarded write process. However, Jones et al. also state that, "In the following descriptions of fragment operations, snapshots of the request queue for each stage in the process will be provided."[28] Jones et al. appear to teach a request queue. The cited text and the remaining text of Jones et al. do not appear to teach or suggest that the request queue holds a plurality of threads of sequential commands that exist simultaneously. Therefore, Krakirian and Jones et al. alone, or in combination, do not appear to teach or suggest (item 7) a data control having a command queuing engine that creates a plurality of threads of sequential commands that exist simultaneously as presently claimed.

In summary, (item 6) a prima facie case has not been established showing motivation to combine the teachings of Krakirian with Jones et al. Furthermore, the proposed combination still does not appear to teach or suggest (item 7) a data control having a command queuing engine that creates a plurality of threads of sequential commands that exist simultaneously as presently claimed. As such, the pending claim 3 is fully patentable over the cited references and the rejection should be reversed.

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[28] Jones et al., column 40, lines 21-23.

Selected groupings of the claims are each patentable over Krakirian in view of Jones et al. and Bean et al.

2. Group 4 (Claims 16-20) are fully patentable over Krakirian in view of Jones et al. and Bean et al.

A prima facie case has not established that it would have been obvious to one of ordinary skill in the art to modify the teaching of Krakirian with the teaching of Jones et al. and Bean et al. In particular, the burden of proof has not been meet to show motivation to modify Krakirian with Jones et al. and Bean et al. Krakirian teaches a system for storing initiator, queue tag, and logical block information, disconnecting from target if command is not auto transfer, reconnecting and performing data transfer (Title). Jones et al. teach a system for scheduling read ahead operations if new request is within a proximity of N last read requests wherein N is dependent on independent activities (Title). Bean et al. teach an apparatus and method for controlling digital data processing system employing multiple processors (Title).

Presently pending claims 16-20 depend from presently pending claim 3 and therefore, contains all of the limitations of pending claim 3 Consequently, the arguments presented above in support of the patentability of pending claim 3 are incorporated hereunder in support of pending claims 16-20.

The Examiner has argued that motivation to combine the teachings of Krakirian, Jones et al. and Bean et al. arises for an increased efficiency of the Krakirian and Jones et al's microprocessor.[29] Such a conclusory statement alone is not thorough and searching evidence. No evidence has been provided why one of ordinary skill in the art would believe that the proposed

[29] Office Action, June 18, 2002, page 6, lines 2-3.

combination of Krakirian and Jones et al. should have an increased microprocessor efficiency. No evidence has been provided why one of ordinary skill in the art would seek Bean et al. in particular to *increase* the microprocessor efficiency of the proposed combination. No evidence has been provided that the teaching of Bean et al. would have a reasonable expectation of success to increase the efficiency of the microprocessor in the proposed combination. Finally, no indication has been provided as to which parameter or parameters of the proposed Krakirian and Jones et al. combined microprocessor would be made more efficient by the teaching of Bean et al.

Furthermore, the United States patent laws allow improvements to existing inventions to be patented.[30] A desire to improve an invention alone is not sufficient motivation to make a combination obvious. Therefore, (item 8) a prima facie case of obviousness to combine Krakirian with Jones et al. and Bean et al. has not been established for lack of motivation. As such, the pending claims 16-20 are fully patentable over the cited references and the rejection should be reversed.

Selected groupings of the claims are each patentable over Krakirian in view of Bean et al.

3. Group 4 (Claims 23-25) are fully patentable over Krakirian in view of Bean et al.

A prima facie case has not established that it would have been obvious to one of ordinary skill in the art to modify the teaching of Krakirian with the teaching of Bean et al. In particular, the burden of proof has not been meet to show motivation to modify Krakirian with Bean et al. Krakirian teaches a system for storing initiator, queue tag, and logical block information,

[30] 35 U.S.C. §101.

disconnecting from target if command is not auto transfer, reconnecting and performing data transfer (Title). Bean et al. teach an apparatus and method for controlling digital data processing system employing multiple processors (Title).

Presently pending claims 23-25 depend from presently pending claim 21 and therefore, contains all of the limitations of pending claim 21. Consequently, the arguments presented above in support of the patentability of pending claim 21 are incorporated hereunder in support of pending claims 23-25.

The Examiner has argued that motivation to combine the teachings of Krakirian and Bean et al. arises to increase efficiency of the Krakirian microprocessor.[31] Such a conclusory statement alone is not thorough and searching evidence. No evidence has been provided why one of ordinary skill in the art would believe that the microprocessor of Krakirian should have an increased efficiency. No evidence has been provided why one of ordinary skill in the art would seek Bean et al. in particular to *increase* the microprocessor efficiency. No evidence has been provided that the teaching of Bean et al. would have a reasonable expectation of success to increase the efficiency of the Krakirian microprocessor. Finally, no indication has been provided as to which parameter or parameters of the proposed microprocessor would be made more efficient by the teaching of Bean et al.

Furthermore, the United States patent laws allow improvements to existing inventions to be patented.[32] A desire to improve an invention alone is not sufficient motivation to make a combination obvious. Therefore, (item 9) a prima facie case of obviousness to combine Krakirian

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[31] Office Action, June 18, 2002, page 6, lines 9-10.

[32] 35 U.S.C. §101.

with Bean et al. has not been established for lack of motivation. As such, the pending claims 23-25 are fully patentable over the cited references and the rejection should be reversed.

Groups 1-5 are separately patentable.

During prosecution, each claim is to be analyzed separately for patentability against 35 U.S.C. §112 compliance.[33] As such, each of the above groups may be considered to be separately patentable over every other group. The arguments provided above for each claim are listed in Table I by item number as follows:

TABLE I

Claim	Item Number								
	1	2	3	4	5	6	7	8	9
3						Group 3	Group 3		
16						Group 4	Group 4	Group 4	
17						Group 4	Group 4	Group 4	
18						Group 4	Group 4	Group 4	
19						Group 4	Group 4	Group 4	
20						Group 4	Group 4	Group 4	
21	Group 1	Group 1	Group 1						
22	Group 1	Group 1	Group 1						
23	Group 5	Group 5	Group 5						Group 5
24	Group 5	Group 5	Group 5						Group 5
25	Group 5	Group 5	Group 5						Group 5
26				Group 2	Group 2				

[33] M.P.E.P. §2163.

Each group has a unique set of arguments. Therefore, even if all rejections where to be upheld in any particular group, one or more different rejections may be reversed in the other groups allowing for independent patentability of each group. For example, the rejection of group 3 may be upheld if the arguments for items 6 and 7 are found unpersuasive. However, the rejection of group 4 may be reversed on the argument for item 8, allowing for independent patentability of group 4 over group 3. Similar reasoning may be found for the independent patentability of each group over every other group.

C. CONCLUSION

The Krakirian reference does not appear to anticipate every element as arranged in the pending claims 21, 22 and 26. In particular, Krakirian does not appear to disclose or suggest a data controller that (a) minimizes interrupts to a processor by (b) reordering a plurality of commands received from a host computer and (c) a data controller that creates threads of a plurality of commands as presently claimed. The Examiner has admitted that the queue disclosed by Krakirian cannot hold plural threads simultaneously.

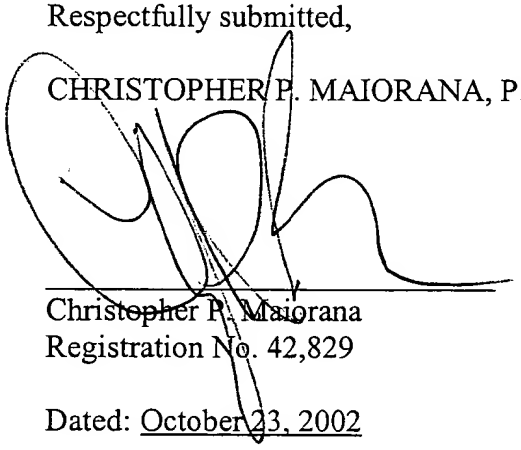
The Krakirian reference in view of the Jones et al. reference does not appear to teach or suggest every element as arranged in the pending claim 3. In particular, Krakirian and Jones et al. alone, or in combination, do not appear to teach or suggest a data control having a command queuing engine that creates a plurality of threads of sequential commands that exist simultaneously as presently claimed. In addition, a prima facie case has not been made that the pending claims are obvious over the cited references. In particular, the burden of proof has not been meet to show

motivation to combine (a) Krakirian with Jones et al., (b) Krakirian with Jones et al. and Bean et al., and (c) Krakirian with Bean et al.

It is respectfully requested that the Board overturn the Examiner's rejections of pending claims 3 and 16-26 and hold that the claims are not rendered anticipated or obvious by the cited references. However, should the Board find the arguments herein in support of independent claims 3, 21 and/or 26 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Christopher P. Maiorana
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Dated: October 23, 2002

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IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

3. A data controller, that is couplable to a host and coupled to a storage medium, microprocessor, local storage and a buffer memory, comprising a command queuing engine that creates a plurality of threads of sequential commands that exist simultaneously while minimizing interrupts associated to the commands.

16. The data controller of claim 3 wherein the command queueing engine includes a transfer extend generator that generates transfer extend entries.

17. The data controller of claim 16 wherein the transfer extend generator is coupled to the buffer memory to store the transfer extend entries.

18. The data controller of claim 3 wherein the command queuing engine includes a data retrieval channel.

19. The data controller of claim 18 wherein the command queueing engine further includes a status retrieval channel.

20. The data controller of claim 18 wherein the data retrieval channel is coupled to the buffer memory to retrieve transfer extend entries and to return used read pointers.

21. A data controller of a peripheral device having a storage medium and a processor, wherein the data controller minimizes interrupts to the processor by re-ordering a plurality of commands received from a host computer from an order of arrival into an order of sequence in the storage medium.

22. The data controller of claim 21, further comprising a command queueing engine configured to arrange the plurality of commands into at least one thread.

23. The data controller of claim 22, wherein the command queueing engine comprises:

a transfer extend generator configured to generate transfer extend entries for a data transfer between the storage medium and a host computer; and

a data retrieval channel coupled to receive the transfer extend entries for programming the data transfer.

24. The data controller of claim 23, wherein the command queueing engine further comprises a status retrieval channel.

25. The data controller of claim 24, wherein each of the retrieval channels are coupled to receive transfer extend entries and to provide used read pointers to a first storage device of the peripheral device.

26. A peripheral device that includes a data controller, a microprocessor, a buffer memory, local memory and a storage medium, and that is couplable to a host, wherein the data controller creates threads of a plurality of commands and generates interrupts at the beginning and end of the plurality of commands relative to a data transfer.